

CLAIMS

What is claimed is:

- 1 1. A method of optimizing level converter placement, said method comprising the
2 steps of:
 - 3 a) selectively placing each level converter at a minimum power point to
4 minimize net power and transitional delay, transitional delay being a first voltage net
5 delay to said level converter, through said level converter and a second voltage net delay
6 from said level converter; and
 - 7 b) eliminating inefficient level converters.
- 1 2. A method as in claim 1, wherein at least one said minimum power point is located
2 at a geometric center between a pair of sinks on a corresponding second voltage net.
- 1 3. A method as in claim 1, wherein at least one first voltage net originates at a first
2 quadrant and a corresponding second voltage net connects to a plurality of sinks in a
3 second quadrant and said minimum power point is located at minimum horizontal (x) and
4 vertical (y) coordinates of said plurality of sinks.
- 1 4. A method as in claim 1 at least one first voltage net originates at a first quadrant
2 and a corresponding second voltage net connects to a plurality of sinks in a second
3 quadrant and wherein said minimum power point is located comprising the steps of:
 - 4 A) locating a weighted center of said plurality of sinks; and
 - 5 B) providing a projection from said weighted geometric center to a baseline
6 intersecting one of said plurality of sinks.

- 1 5. A method as in claim 4 wherein said baseline is on a diagonal with axes of said
2 second quadrant and said intersecting one is closest to said axes.
- 1 6. A method as in claim 4 wherein locating said minimum distance comprises
2 finding a location at a Manhattan distance from a closest one of said plurality of sinks to
3 a source driving said first voltage net.
- 1 7. A method as in claim 1, wherein at least one first voltage net originates at a first
2 quadrant and a corresponding second voltage net connects to a plurality of sinks in a
3 second quadrant and third quadrant and said minimum power point is located at a side
4 drive point.
- 1 8. A method as in claim 7, wherein said second quadrant and said third quadrant are
2 on one side of an axis, at least one of said plurality of sinks being at a least distance from
3 said axis and said side drive point being located at said least distance directly across said
4 axis from a driver driving said at least one first voltage net.
- 1 9. A method as in claim 1, wherein at least one first voltage net originates at a first
2 quadrant and a corresponding second voltage net connects to a plurality of sinks in a
3 second quadrant and third quadrant and said minimum power point is located at a source
4 driving said first voltage net.
- 1 10. A method as in claim 1, wherein at said minimum power point is selected to
2 minimize wiring.
- 1 11. A method as in claim 1 wherein the step (b) of eliminating inefficient level
2 converters comprises deleting level converter fanin cones below a selected minimum
3 cone size.

1 12. A method as in claim 1 wherein the step (b) of eliminating inefficient level
2 converters comprises the steps of:

- 3 i) defining fanin cones for each of said level converters;
- 4 ii) reverting first voltage level nets in fanin cones below a selected minimum
5 fanin size.

1 13. A method as in claim 12, wherein the step (ii) of reverting voltage level nets
2 comprises:

- 3 A) selecting a smallest fanin cone size;
- 4 B) reverting said first voltage level nets having said smallest fanin cone size;
- 5 C) re-defining said fanin cones;
- 6 D) returning to step (A) until said smallest fanin cone size selected in step (A)
7 is said selected minimum fanin cone size.

1 14. A method as in claim 1 wherein the step (b) of eliminating inefficient level
2 converters comprises the steps of:

- 3 i) identifying second voltage level circuit elements receiving inputs from at
4 least two of said level converters;
- 5 ii) converting selected ones of said second voltage circuit elements to an
6 equivalent first voltage circuit element;
- 7 iii) deleting said at least two level converters; and
- 8 iv) inserting a level converter at each output of said equivalent first voltage
9 circuit element.

1 15. A method as in claim 14, wherein said second voltage circuit elements are
2 selected in step (ii) by checking timing through said equivalent first voltage circuit
3 element and said level converter at each output.

1 16. A method as in claim 1, wherein the step (b) of eliminating inefficient level
2 converters comprises selectively replacing first voltage level buffer and level converter
3 pairs with a single said level converter, said pairs being one said first voltage level buffer
4 driving a corresponding said level converter.

1 17. A method as in claim 16, wherein said pairs are selected by checking timing
2 through said single level converter.

1 18. A method as in claim 1, wherein an input netlist, technology definition and timing
2 constraints are provided for placing and wiring step (a).

1 19. A method of optimizing level converter placement in a multi supply integrated
2 circuit design, said method comprising the steps of:

3 a) providing an input netlist, technology definition and timing constraints for
4 a circuit design;

5 b) selectively placing level converters to minimize net power and transitional
6 delay in said circuit design, each of said level converters being placed at a corresponding
7 minimum power point, transitional delay being a first voltage net delay to a level
8 converter, through said level converter and a second voltage net delay from said level
9 converter; and

10 c) deleting level converter fanin cones for corresponding said level
11 converters below a selected minimum cone size;

12 d) converting selected second voltage level circuit elements receiving inputs
13 from at least two of said level converters to an equivalent first voltage circuit element;
14 and

15 e) selectively replacing first voltage level buffer and level converter pairs
16 with a single said level converter, said pairs being one said first voltage level buffer
17 driving a corresponding said level converter.

1 20. A method as in claim 19, wherein selectively placing said level converters in step
2 (b) comprises:

3 i) identifying ones of said level converters driving pairs of sinks on a
4 corresponding second voltage net and locating said minimum power point for said pair at
5 a geometric center between said pair;

6 ii) identifying first voltage nets originating at a first quadrant with
7 corresponding second voltage nets connecting to a plurality of sinks in a second quadrant
8 and locating said minimum power point in said second quadrant; and

9 iii) identifying said first voltage nets originating at a first quadrant with a
10 corresponding second voltage net connecting to a plurality of sinks in a second quadrant
11 and third quadrant and locating said minimum power point with said sinks.

1 21. A method as in claim 20, wherein said minimum power point is located in step (ii)
2 at minimum horizontal (x) and vertical (y) coordinates of said plurality of sinks.

1 22. A method as in claim 20, wherein, wherein said minimum power point is located
2 in step (ii) comprising the steps of:

3 A) locating a weighted center of said plurality of sinks; and

4 B) providing a projection from said weighted geometric center to a baseline
5 intersecting one of said plurality of sinks.

1 23. A method as in claim 22, wherein said baseline is on a diagonal with axes of said
2 second quadrant and said intersecting one is closest to said axes.

1 24. A method as in claim 22, wherein locating said minimum distance comprises
2 finding a location at a Manhattan distance from a closest one of said plurality of sinks to
3 a source driving said first voltage net.

1 25. A method as in claim 20, wherein said minimum power point is located in step
2 (iii) at a side drive point.

1 26. A method as in claim 25, wherein locating said side drive point comprises:
2 A) locating an axis between a driver driving a transitional net and sinks on
3 said transitional net;
4 B) locating at least one of said sinks at a least distance from said axis; and
5 C) locating a point at said least distance directly across said axis from said
6 driver.

1 27. A method as in claim 20, wherein said minimum power point is located in step
2 (iii) at a source driving said first voltage net.

1 28. A method as in claim 19, wherein the step (c) of deleting fanin cones comprises
2 the steps of:
3 i) defining fanin cones for each of said level converters;
4 ii) reverting first voltage level nets in fanin cones below a selected minimum
5 fanin size.

1 29. A method as in claim 28, wherein the step (ii) of reverting voltage level nets
2 comprises:
3 A) selecting a smallest fanin cone size;
4 B) reverting said first voltage level nets having said smallest fanin cone size;
5 C) re-defining said fanin cones;
6 D) returning to step (A) until said smallest fanin cone size selected in step (A)
7 is said selected minimum fanin cone size.

1 30. A method as in claim 19, wherein said second voltage circuit elements are
2 selected in step (d) by checking timing through said equivalent first voltage circuit
3 element and said level converters placed at each output.

1 31. A computer program product for optimizing level converter placement in a multi
2 supply integrated circuit (IC) design, said computer program product comprising a
3 computer usable medium having computer readable program code thereon, said computer
4 readable program code comprising:

5 computer program code means for locating a minimum power point to minimize
6 power and transitional delay for a level converter placed at said minimum power point,
7 transitional delay being a first voltage net delay to said level converter, through said level
8 converter and a second voltage net delay from said level converter

9 computer program code means for placing level converters at minimum power
10 points; and

11 computer program code means for eliminating inefficient said level converters.

1 32. A computer program product as in claim 31, wherein the computer program code
2 means for locating said minimum power point comprises:

3 computer program code means for locating a geometric center of a plurality of
4 circuit sink elements on a net;

5 computer program code means for locating a weighted center of said plurality of
6 circuit sink elements on said net; and

7 computer program code means for determining bounds for said plurality of circuit
8 sink elements on said net.

1 33. A computer program product as in claim 32, wherein the computer program code
2 means for locating said minimum power point further comprises:

3 computer program code means for providing a projection from said weighted
4 geometric center to a baseline intersecting one of said plurality of sinks.

1 34. A computer program product as in claim 33, wherein the computer program code
2 means for locating said minimum power point further comprises:
3 computer program code means for finding a location at a Manhattan distance from
4 a closest one of said plurality of sinks to a source driving said first voltage net.

1 35. A computer program product as in claim 31, the computer program code means
2 for eliminating inefficient level converters comprising:
3 computer program code means for identifying and deleting level converter fanin
4 cones for corresponding said level converters below a selected minimum cone size;
5 computer program code means for identifying and converting selected second
6 voltage level circuit elements receiving inputs from at least two of said level converters to
7 an equivalent first voltage circuit element; and
8 computer program code means for selectively replacing first voltage level buffer
9 and level converter pairs with a single said level converter, said pairs being one said first
10 voltage level buffer driving a corresponding said level converter.

1 36. A computer program product as in claim 35, wherein the computer program code
2 means for locating said identifying and deleting fanin cones comprises:
3 computer program code means for reverting first voltage level nets in fanin cones
4 below a selected minimum fanin size.

1 37. A computer program product as in claim 35, wherein the computer program code
2 means for reverting voltage level nets comprises:
3 computer program code means for selecting a smallest fanin cone size;
4 computer program code means for reverting said first voltage level nets having
5 said smallest fanin cone size; and
6 computer program code means for re-defining said fanin cones.

1 38. A computer program product as in claim 31, further comprising:
2 computer program code means for receiving an input netlist, technology
3 definition and timing constraints.